**Experiment 4: Mux and Demux in Verilog**

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**AIM**

(a) Development of Verilog modules for a 4x1 MUX.

**VERILOG CODE**

**Data flow level**

module mux(

input wire s0,s1,i0,i1,i2,i3,

output wire y);

assign y = (~s0)&(~s1)&i0 | (s0)&(~s1)&i1| (~s0)&(s1)&i2 | (s0)&(s1)&i3;

endmodule

**Testbench**

`timescale 1ns/1ps

module test\_mux;

reg t\_s0,t\_s1,t\_i0,t\_i1,t\_i2,t\_i3;

wire t\_y;

mux uut(.s0(t\_s0),.s1(t\_s1),.i0(t\_i0),.i1(t\_i1),.i2(t\_i2),.i3(t\_i3),.y(t\_y));

initial

begin

$dumpvars(1,test\_mux);

t\_s1=1'b0;

t\_s0=1'b0;

t\_i0=1'b1;

t\_i1=1'b0;

t\_i2=1'b1;

t\_i3=1'b0;

#10;

t\_s1=1'b0;

t\_s0=1'b1;

t\_i0=1'b1;

t\_i1=1'b0;

t\_i2=1'b1;

t\_i3=1'b0;

#10;

t\_s1=1'b1;

t\_s0=1'b0;

t\_i0=1'b1;

t\_i1=1'b0;

t\_i2=1'b1;

t\_i3=1'b0;

#10;

t\_s1=1'b1;

t\_s0=1'b1;

t\_i0=1'b1;

t\_i1=1'b0;

t\_i2=1'b1;

t\_i3=1'b0;

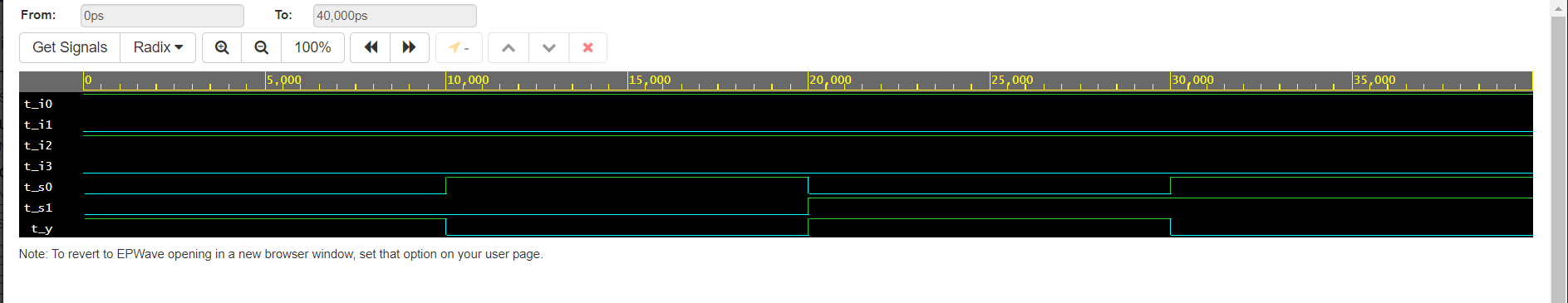
#10;

$stop;

end

endmodule

**Output**



**AIM**

(b) Development of Verilog modules for a 1x4 DEMUX.

**VERILOG CODE**

**Data flow level**

module demux(

input wire s0,s1,d,

output wire y0,y1,y2,y3);

assign y0 = (~s1)&(~s0)&d;

assign y1 = (~s1)&(s0)&d;

assign y2 = (s1)&(~s0)&d;

assign y3 = (s1)&(s0)&d;

endmodule

**Testbench**

`timescale 1ns/1ps

module test\_demux;

reg t\_s0,t\_s1,t\_d;

wire t\_y0,t\_y1,t\_y2,t\_y3;

demux uut(.s0(t\_s0),.s1(t\_s1),.d(t\_d),.y0(t\_y0),.y1(t\_y1),.y2(t\_y2),.y3(t\_y3));

initial

begin

$dumpvars(1,test\_demux);

t\_s0=1'b0;

t\_s1=1'b0;

t\_d=1'b1;

#10;

t\_s0=1'b1;

t\_s1=1'b0;

t\_d=1'b1;

#10;

t\_s0=1'b0;

t\_s1=1'b1;

t\_d=1'b1;

#10;

t\_s0=1'b1;

t\_s1=1'b1;

t\_d=1'b1;

#10;

$stop;

end

endmodule

**Output**

